REMARKS

Reconsideration and allowance of the present application based on the following remarks is respectfully requested.

Claim 47 is amended. Claims 48–57 are added. Claims 1–57 are pending in the application.

Rejection under 35 U.S.C. § 112

Claims 44–47 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification. In light of the following remarks, applicant respectfully requests that this rejection be withdrawn.

The following indicates one example of how the claimed feature "wherein a frequency of the display signal is based on an amount of the video data that has not yet been read from the buffer" is disclosed and illustrated in the specification as originally filed:

The specification discloses a write pointer that may be associated with operations of writing video data to a buffer (e.g. Figure 2 at block 203). For example, the specification discloses that in some embodiments, a write pointer may be updated at each write operation (p. 7, l. 25). Therefore, the specification discloses that a write pointer may be related to video data written to a buffer.

Likewise, the specification discloses a read pointer that may be associated with operations of reading the video data from the buffer (e.g. Figure 2 at block 205). For example, the specification discloses that in some embodiments, a read pointer may be updated at each read operation (p. 8, l. 4). Therefore, the specification discloses that a read pointer may be related to the portion of the video data that has been read from the buffer.

The specification discloses that the pointers may be updated with information expressed in terms of bytes (p. 8, ll. 20–25). Therefore, a write pointer may be updated according to a number of bytes of video data written to a buffer, and a read pointer may be updated according to a number of bytes of the video data read from the buffer.

The specification also discloses comparing a write pointer and a read pointer (e.g. Figure 2 at block 206). As a result of the updating in terms of bytes, the write pointer may

indicate a number of bytes of video data written to a buffer, and the read pointer may indicate a number of bytes of the video data read from the buffer (e.g. modulo a buffer size). Therefore, the specification discloses comparing a number of bytes of video data written to a buffer with a number of bytes of the video data read from the buffer.

Clearly, such a comparison provides information relating to the amount of the video data not yet read from the buffer:

- The result of the comparison may be a match; this result indicates that the amount not yet read is zero (e.g. same number of bytes written and read).
- The result of the comparison may be "greater than" or some equivalent; this result indicates that the amount not yet read is positive (e.g. more bytes written than read).
- The result of the comparison may be "less than" or some equivalent; this result indicates that the amount not yet read is negative (e.g. fewer bytes written than read).
- The comparison may be implemented as a difference, in which case the result may indicate the number of data bytes not yet read from the buffer.

In each of these examples, the comparison result is based on an amount of the video data not yet read from the buffer. Therefore, the specification discloses obtaining a result based on an amount of the video data that has not yet been read from the buffer.

The specification teaches that a read frequency may be dynamically adjustable responsive to a comparison of the write and read pointers (p. 8, ll. 4–6, see also block 222 of Figure 2). For example, based on the comparison result, a buffer overflow or underflow condition may be detected (e.g. Figure 2 at block 221), and such condition may be indicated for appropriate action. As demonstrated above, the comparison result may be based on an amount of the video data not yet read from the buffer. Therefore, at least for the reasons set forth above, support for the claim phrase "wherein a frequency of the display signal is based on an amount of the video data that has not yet been read from the buffer" is disclosed and illustrated in the specification as filed.

Rejection under 35 U.S.C. § 102

Claims 1–47 were rejected under 35 U.S.C. § 102(b) as being anticipated by Shimizu et al. (U.S. Patent No. 5,861,879). In light of the following remarks, applicant respectfully requests that this rejection be withdrawn.

Claim 1 recites reading source data from a buffer, comparing a write pointer and a read pointer, and adjusting a frequency of the reading responsive to the comparing.

Claims 12 and 31 recite a frequency controller configured to indicate a reading frequency based on a determined relation between a value of a write pointer and a value of a read pointer.

Claim 21 recites adjusting a display frequency in accordance with a detected condition.

Claim 38 recites adjusting a display frequency responsive to a comparison of a write pointer and a read pointer.

Claim 44 recites that a frequency of a display signal is based on an amount of video data not yet read from a buffer.

The Examiner states that Shimizu discloses an address observation circuit 16 that indicates a reading frequency based on a determined relation between a value of a write pointer and a value of a read pointer. Applicant respectfully notes that the cited portions of Shimizu (Figures 2–6 and col. 5, l. 29 – col. 8, l. 57) do not teach any indication of a reading frequency based on such a relation. Indeed, applicant finds no such teaching anywhere in Shimizu.

Shimizu teaches writing an input video signal into alternate field memories M1 and M2 (see abstract and Figure 2). Write enable signals WE1, WE2 control the writing operation, such that the input video signal is alternately written into one field memory or the other (col. 5, ll. 47–53).

Shimizu also teaches reading a display video signal alternately from field memories M1 and M2 (see abstract and Figure 2). Read enable signals RE1, RE2 control the reading operation, such that the display video signal is alternately read from one field memory or the other (col. 6, ll. 14–16).

An address observation circuit judges whether a read address passes by a write address (see abstract and Figure 2). If such a condition is judged, then the address observation circuit outputs a MON signal (col. 6, l. 65 – col. 7, l. 2), and the same read memory is accessed for reading (abstract). In this way, one of the field memories is read twice for two field periods (col. 7, ll. 5–7; see also col. 6, l. 42 – col. 7, l. 26: section labeled "Switching of reading from between Memories M1 and M2").

As noted above, Shimizu uses the labels RE1, RE2 to indicate read enable signals, not to indicate any frequency. The label R MEMORY is used in Figure 6 to indicate the field memory currently used for reading (see col. 7, ll. 61–64; col. 8, ll. 33–38), not to indicate any frequency. As noted above, Shimizu uses the label MON to indicate a signal "used for switching between the field memories M1 and M2 to determine a read memory" (col. 6, ll. 35–37), not to indicate any frequency.

In the system of Shimizu, the vertical and horizontal synchronizing signals of the display video signal are based on a read clock RCLK generated by display video clock generator 14 (col. 6, ll. 5–18). The read clock RCLK may be generated in synchronism with display V and H signals that are externally input (col. 6, ll. 25–29). The cited portions of Shimizu do not teach or otherwise suggest any indication of a reading frequency or a display frequency based on a determined relation or comparison between pointer values.

At least for the reasons set forth above, applicant respectfully submits that claims 1–47 are allowable over the art of record.

New claims

Claims 48–56 are newly presented. Claims 48, 50, 52, 54, and 56 relate to selection of a frequency from among a range of supported refresh rates. Support for these claims may be found at, e.g., page 1, line 28 to page 2, line 5; and page 4, lines 18–26 of the specification as filed.

Claims 49, 51, 53, 55, and 57 relate to scaling data to correspond to a predetermined pixel array size. Support for these claims may be found at, e.g., page 1, line 28 to page 2, line 5; page 6, lines 1–19; and page 9, lines 13–26 of the specification as filed.

In view of the foregoing, the claims are now believed to be in form for allowance, and such action is hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, he is kindly requested to contact the undersigned at the telephone number listed below.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached Appendix is captioned **"Version with markings to show changes made"**.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

44. (Amended) A method of video signal processing, said method comprising:

writing video data to a buffer;

reading a portion of the video data from the buffer; and

transferring a display signal based on the portion of the video data to a display device,

wherein a frequency of the display signal is based on an amount of the video data that has not yet been read from the buffer.